Low Power 4×4 Bit Multiplier Design using Dadda Algorithm and Optimized Full Adder

Muhammad Hussnain Riaz [1,*], Syed Adrees Ahmed [1*], Qasim Javaid [1*], Tariq Kamal[2]

Abstract- This paper presents the model of 4-bit multiplier having low power and high speed using Algorithm named Dadda and the basic building block used is optimized Full adder having low power dissipation and minimum propagation delay. Full and half adder blocks have been designed using pass-transistor logic and CMOS process technology to reduce the power dissipation and propagation delay. We have also applied Dadda algorithm to reduce the propagation delay. The model has been designed using Cadence Virtuoso in 90-nm technology. The proposed multiplier starts its operation at the frequency of 3.83 GHz and its average dynamic power is 184.3 μW at the supply of 1V.

Keywords— Dadda Algorithm, Hybrid Design, Optimized Full Adder, 4×4 Bit Multiplier

I. INTRODUCTION

Multiplication is the basic process which is used in different electronic and in various digital communication applications. Multipliers with low latency and minimum power dissipation are preferred to design an optimized circuit so that maximum throughput can be achieved in minimum response time. Building blocks used in multipliers are a full adder and a half adder. Different design implementations of a full adder and half adder circuits have been used to reduce power and delay in order to design an optimized multiplier circuit which includes pass transistor logic, CMOS process technology, split percentage data-driven logic and CMOS process technology. Besides this, different multiplication algorithms also have been used to achieve optimized power and delay product which includes Dadda, Wallace tree, and Vedic and Booth algorithms. The Recent multiplier used Reduced-sp-D3Lsum Adder and Dadda Algorithm technique. This design operates at high frequency and consumes less power as compared to previous designs, but still, power needs to be significantly reduced, so, it will help in the larger circuits where multiplier itself becomes the building block [8]. In proposed work, a multiplier has been designed in which Full adder and half adder has been used as its building block to reduce the power dissipation by using pass-transistor logic and CMOS technology process. Dadda Algorithm has been used to reduce the propagation delay of the multiplier. The paper has been ordered according to this flow. Previous research regarding multiplier and full adder has been presented in Sect. II; proposed research is described in Sect. III; block diagrams and algorithm implementation are covered in Sect. IV and V; results in Sect VI; while the conclusion is in Sect. VII.

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II. PREVIOUS RESEARCH

Different techniques such as; merged delay transformation [1-2], genetic algorithm [3-5], evolutionary algorithm [6], delay path Un-equalization [7], carry-look-ahead logic [8], etc. have been used and implemented to design digital circuits having low power dissipation, minimum delay and to achieve maximum throughput in minimum response time. Techniques include pass-transistor logic CMOS process technology, adiabatic static CMOS logic, reversible logic, etc. Multiplier using Pass transistor logic technique is one which uses a reduced number of transistors and offers small node capacitances which produces minimum delay and increase the speed of the circuit. Multipliers having reversible logic have reduced power dissipation. Multipliers' having adiabatic static CMOS logic produce minimum heat while transferring the charges.

III. PROPOSED RESEARCH

In the proposed research, a modified circuit of the 4*4 multiplier is proposed. This multiplier circuit is based on the optimized full adder which uses 12 transistors i.e., 12T. The design of full adder is hybrid i.e., the design consists of two techniques, pass-transistor logic, and CMOS process technology. Full adder and a half adder as the building block of the circuit have low propagation delay and low power delay product. The power and delay of this full adder are low as compared to other previous designed full adders. This ultimately results in the formulation of multipliers having low propagation delay and minimum power dissipation.

A. DADDA TREE ALGORITHM

Different algorithms have been proposed to decrease the propagation delay during the addition of the partial products generated by AND Gate. One of the most efficient algorithms is Dadda algorithm. The proposed 4*4 multiplier has a total of 16 partial products, so, the height of the tree is four as shown Fig. 1. Dadda Algorithm has been applied for the purpose to reduce the height of the tree from four to two. If we do not apply Dadda algorithm, then we must have to wait for the previous stage to simulate it, because, the next stage uses the carry of the previous stage which will increase the propagation delay. For this simple technique, we have to use the ripple carry adder, it also consumes less power, but the delay is significantly high. To reduce the overall propagation delay of the multiplier Dadda algorithm has been applied.

This is the best technique for reduction in the delay of the overall multiplier design because, at the start, it does not depend on the previous stage. Therefore, the first stage will be implemented without depending on any other stage. First, we have arranged our partial products to make a tree as shown in Fig. 1. These partial products are generated by the AND gate.

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The height of this tree is 4 as the proposed design is the 4-bit multiplier.

B. STAGES OF DADDA ALGORITHM

The objective is to reduce the height of the tree from four to two. Therefore, building blocks have been used in such a way to reduce the tree height from four to three after the completion of first Dadda stage and then from three to two after the completion of the second Dadda Stage. Furthermore, the two Dadda stages are used to reduce this tree. The first and second Dadda stages are shown in Fig. 2 and Fig. 3, respectively.

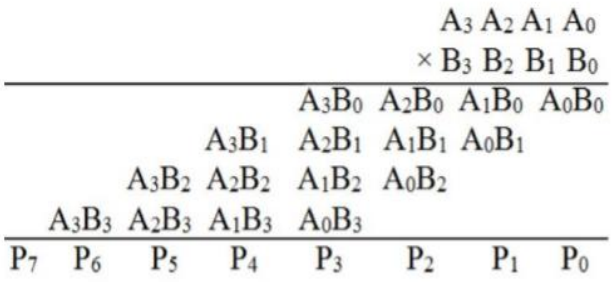

Figure 1: 4 × 4 Multiplications.

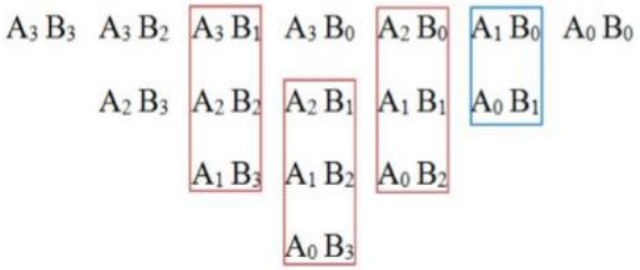

Figure 2: First Dadda Stage

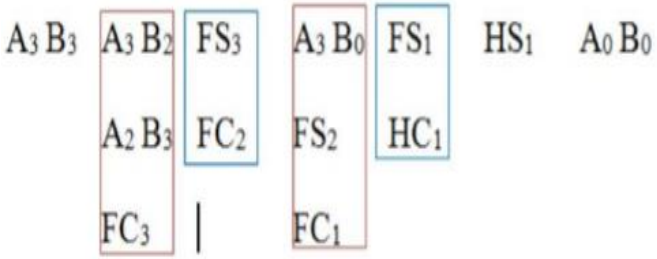

Figure 3: Second Dadda Stage

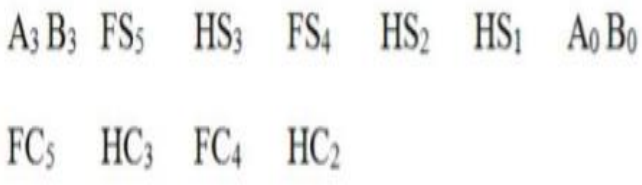

Figure 4: Last Dadda Stage

For a 4*4 tree reduction, stages are as given below

i. First stage with a height of four.
ii. Second stage with a height of three.
iii. Finally, the third stage with a height of two.

C. ALGORITHM IMPLEMENTATION

We apply the Dadda algorithm on this tree to reduce the height of the tree. At the first stage: tree has a height of 4 which we need to reduce by using full adders and half adders. Hence, we have applied a full adder on the 4th column to reduce its height also we have applied half adder on the 2nd column and two more full adders on the 3rd and 5th column to adjust the tree height to 3. Now these HA and FA are working in parallel and no one is dependent on the previous stage. Figure 3 and 4 shows the more tree reduction and in the final stage, we have used a ripple carry adder. The count of the half adder and full adder used in the Dadda stages are given by these formulas

Half adder= H-1 *Full adder=H2-4H+5*

IV. BLOCK DIAGRAM

THE BLOCK DIAGRAM OF OUR PROPOSED MULTIPLIER IS SHOWN IN FIG. 5.

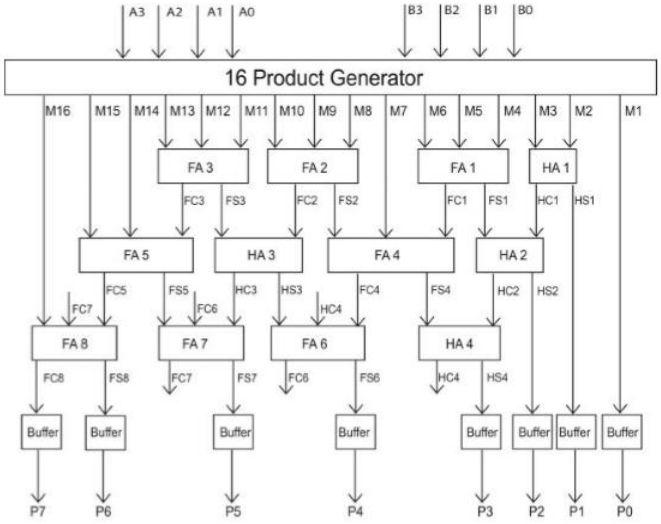

Figure 5: Block Diagram of the proposed Multiplier

The working stages of the proposed model are as follows:

1. In the first step, 16 partial products are generated using AND gate.
2. In the second step, the height of the tree is reduced using Dadda stage using one-half adder (HA) and three full adders (FA).
3. In the third step, the reduction is done by two half adders and two full adders.
4. At last stage of Dadda, we have used a ripple carry adder.
5. Finally, results are passed through the buffer to make the output voltages better (smooth).

V. BUILDING BLOCKS OF PROPOSED MULTIPLIER

THE BLOCKS THAT ARE USED IN THE PROPOSED DESIGN OF MULTIPLIER ARE AS UNDER:

A. *AND GATE*

The proposed model has AND gate for the multiplication of 4*4 multiplier. Consequently, for the 4*4 multiplication, a total of 16 products are generated. Therefore, it has used 16 AND gates for multiplication. The schematic of the AND gate is shown in Fig. 6 while its behavior at different frequencies is shown in table 1. The average dynamic power of AND gate at 5GHz is 7.65µW with a delay of 0.05 nS. The graphical representation of Power delay product (PDP) of AND gate at different frequencies is shown in Fig.7.

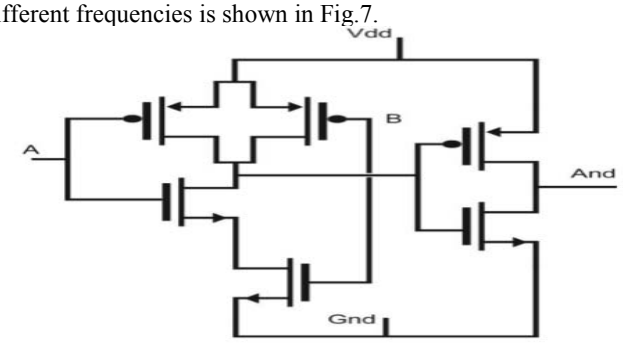

Figure 6: Two input AND gate.

Frequency(GHz)	Power(µW)	Delay(nS)	PDP (fj)
1	1.51	0.034	0.05
2	3.05	0.029	0.08
5	7.65	0.05	0.38

Table 1: AND Gate behavior at different frequencies.

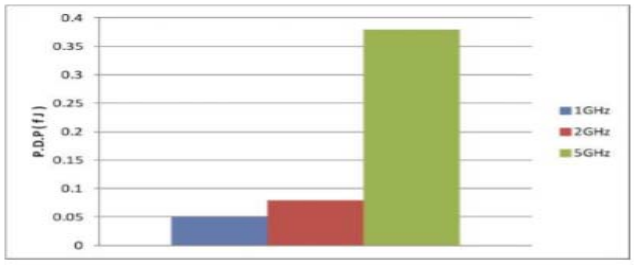

Figure 7: Graphical representation of Power delay product of two input AND gate.

B. *FULL ADDER*

A full adder is a major block in the multiplier. In proposed model Full adder has been modified in order to produce minimum propagation delay and less power dissipation of the circuit, so, that it can further be used to design multiplier having optimized parameters including Power, delay, and less layout area. Proposed modified XOR module in the Full adder is composed of four transistors. The schematic of the proposed XOR module is shown in Fig. 8. We have inverted one input i.e., B input because the B and B' will be used in the next two transistors. We have cascaded a PMOS with NMOS while applying the second input A to the gate terminal of both PMOS and NMOS and instead of connecting the source of the PMOS to Vdd we connected it to the first input B, similarly we have connected the source of the NMOS to the inverted first input i.e., B', which constitutes XOR module. The equation of the XOR module is:

XOR=A'B + AB'

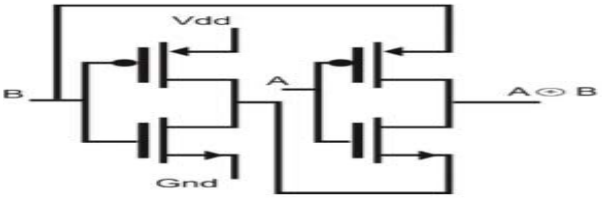

Figure 8: Proposed XOR Module

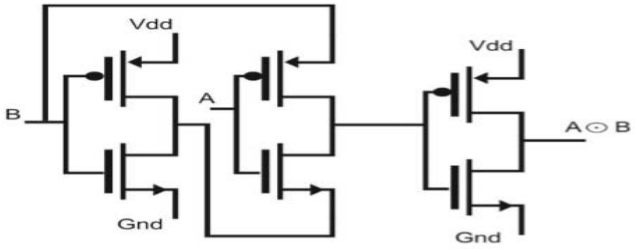

Figure 9: XNOR Module

The XNOR module is shown in Fig.9 by just inverting the output of the XOR module. The equation of the XNOR module is:

XNOR=AB + A'B'

We have inverted this, because, it will be used in the formation of the second XOR module that will generate the Sum of the Full adder. As described above, in that case, we have connected the PMOS source to the XOR module output, while that of NMOS source to the XNOR output. For the generation of carrying we have used two pass transistors. On one pass transistor, we have applied an input C while on the second pass transistor we have applied an input B. The schematic of the full adder is shown in Fig. 10 while its behavior at different frequencies is shown in table 2. The average dynamic power of Full adder at 3GHz is 17.5 µ W with a delay of 0.02 nS.

The equation for the full adder is:

Sum = A ⊕ B ⊕ C Carry = AB + BC + AC

The carry equation if further reduced to If A=B then Carry=A else Carry=C

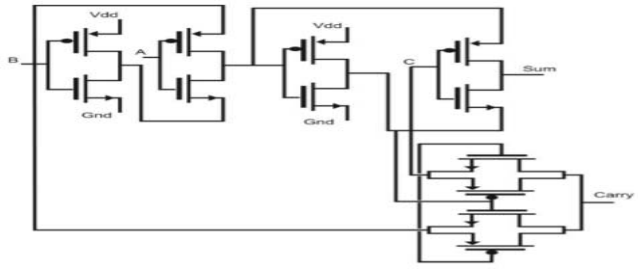

Figure 10: Proposed Full Adder

Frequency(GHz)	Power(µW)	Delay(nS)	PDP (fj)
1	12.96	0.03	0.38
2	15.21	0.02	0.304
3	17.5	0.02	0.35

Table 2: Full Adder behavior at different frequencies

It can be easily shown from the above table that proposed full adder is consuming less power as well as the delay of the proposed full adder is less. The graphical representation of PDP of the full adder at different frequencies is shown in Fig. 11

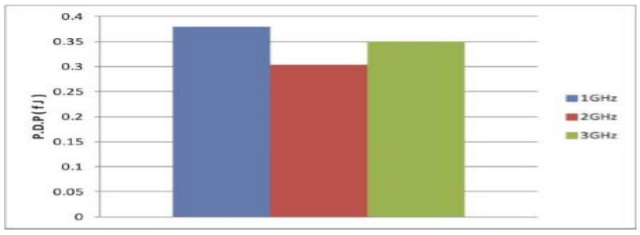

Figure 11: Graphical representation of Power delay product of Full Adder

C. *HALF ADDER*

A half adder is another building block of the multiplier. We used total four half adders in the multiplier design. The schematic of the half adder is shown in Fig. 10, while its behavior at different frequencies is shown in table 3. The average dynamic power of half adder at 3GHz is 9.66µW with a delay of 0.03 nS. The graphical representation of PDP of Half adder at different frequencies is shown in Fig. 13.

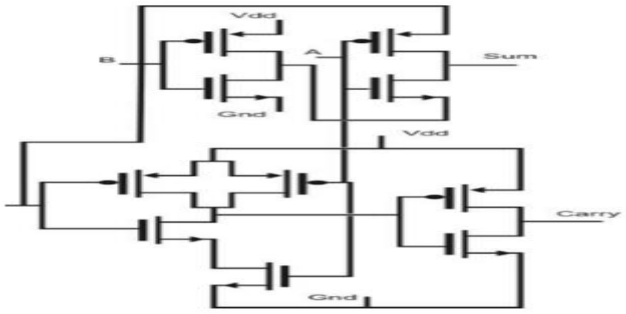

Figure 12: Half Adder

Frequency(GHz)	Power(µW)	Delay(nS)	PDP (fj)
1	3.18	0.05	0.159
2	6.38	0.04	0.255
3	9.66	0.03	0.289

Table 3: Behavior of half adders at different frequencies

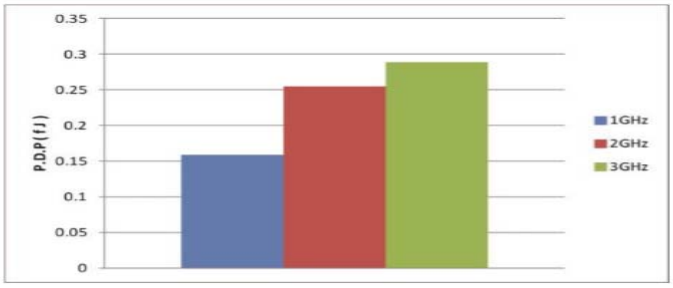

Figure 13: Graphical representation of Power delay product of Half Adder

D. *BUFFER*

The buffer is an amplifier having unity gain. The main function of the buffer is to provide drive capability to pass signals to the final stage. Voltage buffer is used to increase the available current for the circuits having low impedance while retaining the voltage level. On the other hand, current buffers keep the current same and drive the high impedance inputs at higher voltage levels. The average dynamic power of buffer at 3GHz is 6.877µW with a delay of 0.03 nS.

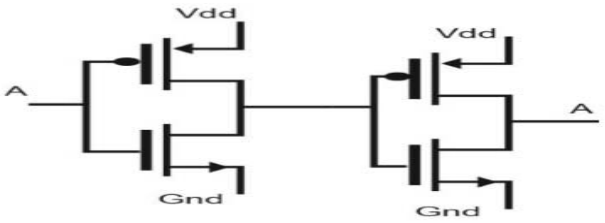

Figure 14: Buffer

VI. RESULTS

For the proposed 4*4 multiplier the inputs A3, A2, A1, A0, B3, B2, B1, and B0 are pulses varying from 0 to 1. The operating frequency of the proposed multiplier is 3.84GHz. The comparison of the proposed multiplier with another multiplier is shown in Table.4.

Design	Technique: Adder	Technique: Multiplier	Delay (ns)	Freq (GHz)	Dynamic Power (µW)	Static Power A=1111 A=0000 B=1111 B=0000 (mW) (µW)	PDP (fJ)
Proposed	Hybrid	Dadda Algorithm	0.09	3.84	184.3	0.015 27.29	16.587
[8]	Reduced Sp-D3Lsum	Dadda Algorithm	0.2620	3.81	623	1.034 59.6	241.826
[6]	Sp-D3Lsum	Dadda Algorithm	0.2942	3.39	1100	1.287 1.04	323.62
[9]	CMOS	Row by Passing	0.6379	1.56	784	1.054 79	500.114

Table 4: Multiplier Behaviour at different Frequencies

Fig. 15 and Fig.16 shows the dynamic power and power delay product comparison of the proposed multiplier with other multiplier designs. It is also shown from the graphical representation that the proposed designed is better in terms of power and PDP. Fig. 17 shows the zoomed portion of the layout of the proposed multiplier. The layout is designed using DSCH 2.6c and Micro wind 2.6a. The layout is verified using the Verilog file generated by the DSCH for the proposed multiplier.

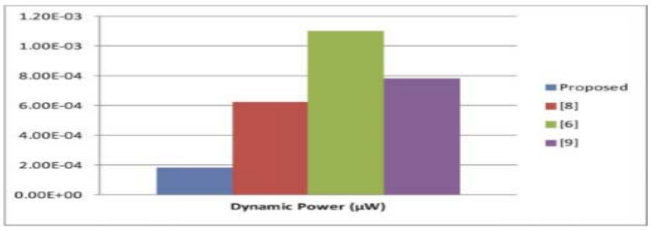

Figure 15: Graphical representation of Dynamic Power of different Multipliers

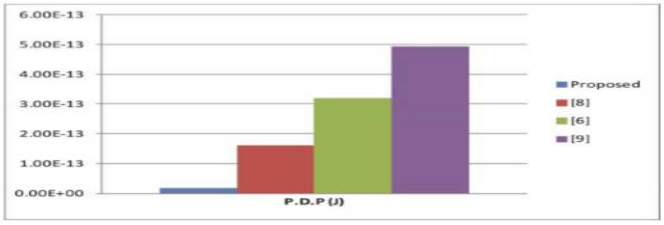

Figure 16: Graphical representation of Power delay product of different Multipliers

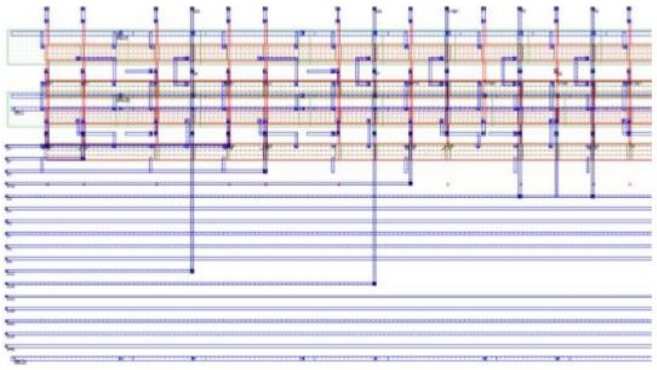

Figure 17: Graphical representation of Dynamic Power of different Multipliers

VII. CONCLUSION

The proposed model having high speed, low latency and minimum delay are being designed which has two modified circuits in it. One is hybrid full adder which has been designed by Pass transistor logic and CMOS process technology. Hybrid full adder has low propagation delay by which maximum throughput can be achieved in minimum response time. A high-speed 4*4 multiplier has been designed using the hybrid Full adder as its building block and Dadda Algorithm has been applied to achieve this. The proposed 4*4 multiplier operates at a frequency of 3.84 GHz and has an average dynamic power of 181.8 μW with a delay of 0.09 nS which is higher as compared to existing multiplier designs. Multiplier having low latency, minimum power dissipation and less layout area have been designed by the proposed model.

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